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S1F76640
Technical Manual

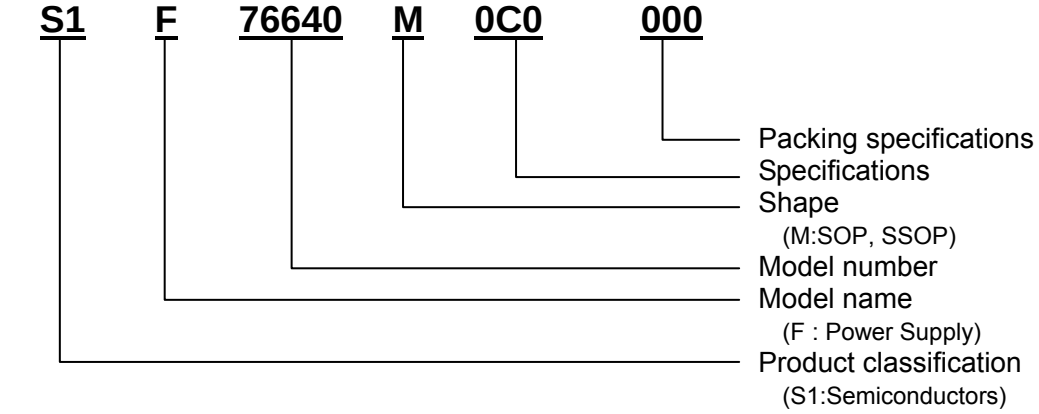
SEIKO EPSON CORPORATION

Rev.1.5

NOTICE

Configuration of product number

●DEVICES



CONTENTS

1. DESCRIPTION

The S1F76640 is a high efficient and low power consuming CMOS DC-DC converter.
It consists of two components: a booster and a stabilizer.
The booster provides double boosting output (3.6 to 11V), triple boosting output (5.4 to 16.5V) or quadruple boosting output (7.2 to 22V) for input voltage (1.8 to -5.5V).
Moreover, the use of external parts such as diode and capacitor provides boosting of higher magnification.
The voltage stabilizer enables you to set to any output voltage.
It also provides three types of negative temperature gradients for voltage stabilization output, and it is most suitable for LCD power.
The S1F76640 enables you to drive an IC (liquid crystal driver, analog IC, etc.) that would usually require another power supply in addition to the logic main power, using a single power supply. Therefore, it is suitable for supplying micro-power to compact electrical devices such as hand-held computers with low power consumption.

2. FEATURES

(1) Highly efficient and low power consuming CMOS DC-DC converter
(2) Easy conversion from input voltage V_{DD} (+3.3V) to three types of positive voltages
Output 2 × V_{DD} (+6.6V), 3 × V_{DD} (+9.9V), and 4 × V_{DD} (+13.2V) from input V_{DD} (+3.3V)
(3) The use of external parts such as diode and capacitor provides boosting of higher magnification
(4) Built-in output voltage stabilizer
- Any output voltage settable with external resistor
(5) Output current: Max. 20mA (V_{DD} = +5V)
(6) Efficiency of power conversion: typ.95 %
(7) Three types of reference voltage with negative temperature gradient characteristics suitable for LCD drive power supply.
(8) Power-off operation by external signal
- Static current for power-off: Max. 2μA
(9) Boosting of higher magnification through serial connection
(10) Low voltage operation: Most suitable for battery drive
(11) Built-in CR oscillation circuit
(12) SSOP2-16 pins
(13) This IC is not designed to be radiation resistant

3. BLOCK DIAGRAM

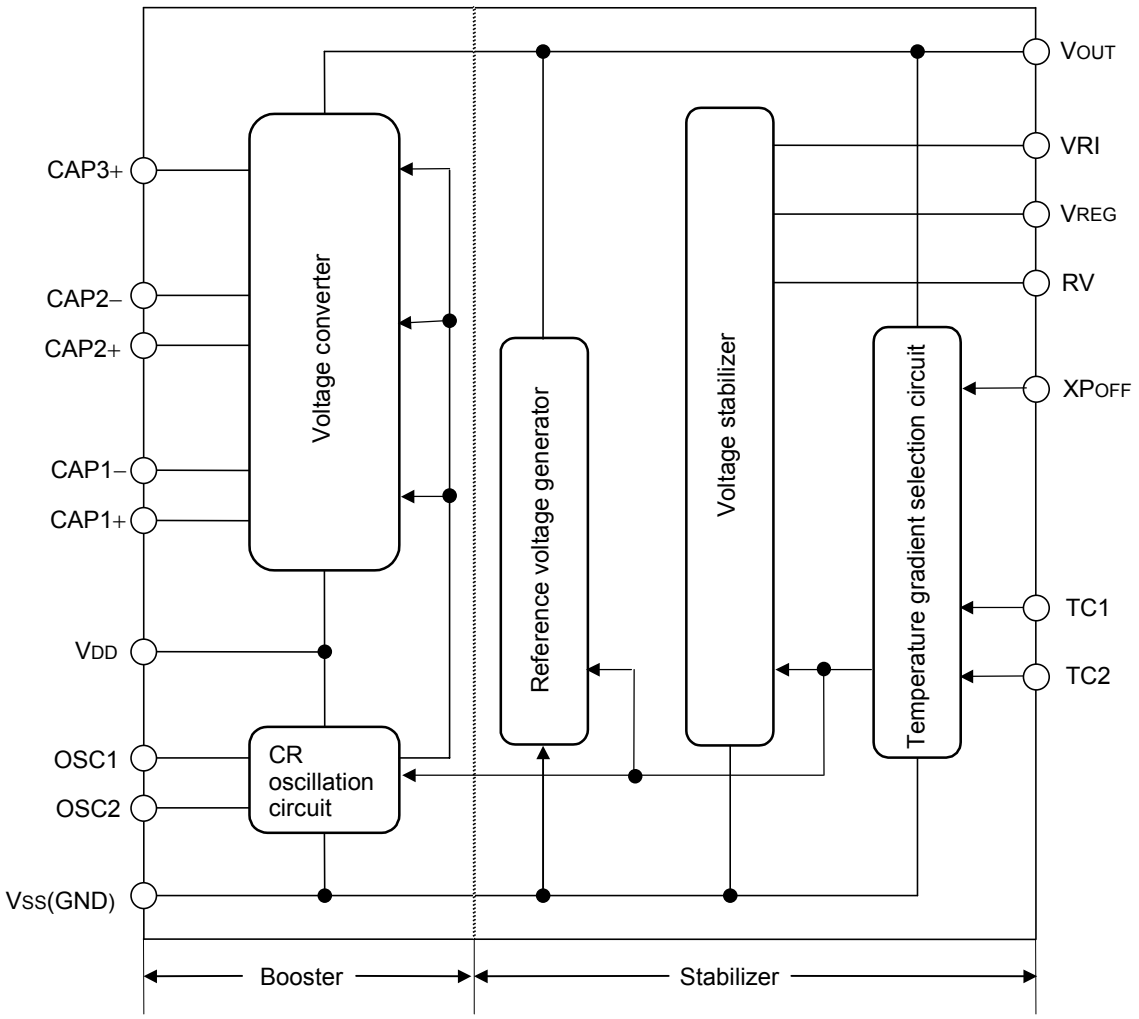


Fig.3.1 Block Diagram

4. PIN DESCRIPTION

4.1 Pin Assignment

SSOP2-16PIN

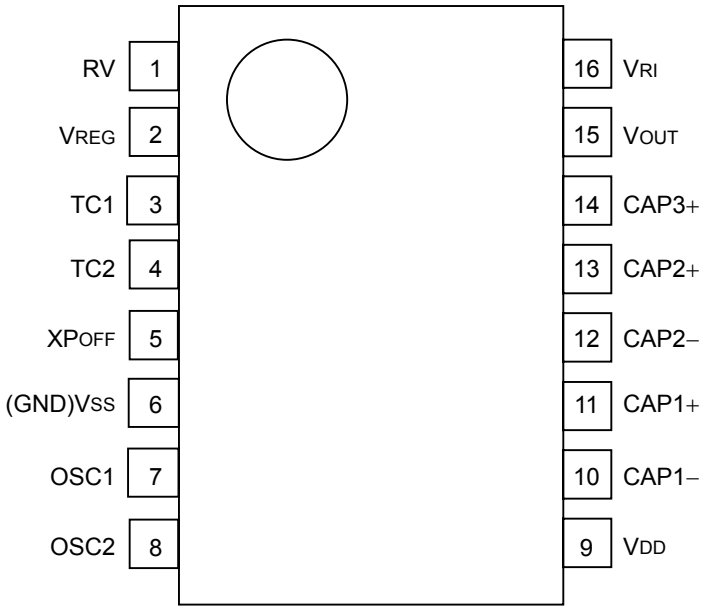


Fig.4.1 SSOP2-16 Pin Assignment

4.2 Pin Functions

Pin Name	Pin No.	Function
CAP1+	11	Positive pin connected to pump-up capacitor for double boosting
CAP1−	10	Negative pin connected to pump-up capacitor for double boosting Next-stage clock for serial connection
CAP2+	13	Positive pin connected to pump-up capacitor for triple boosting
CAP2−	12	Negative pin connected to pump-up capacitor for 3rd boosting Output pin for double boosting (shorted with VOUT)
CAP3+	14	Positive pin connected to pump-up capacitor for quadruple boosting Output pin for triple boosting (shorted with VOUT)
TC1	3	Temperature gradient selection pin
TC2	4	Temperature gradient selection pin
VDD	9	Power supply pin (Positive side, system VCC)
VOUT	15	Output pin for quadruple boosting
VRI	16	Stabilizer input pin
VREG	2	Stabilizing voltage output pin
RV	1	Stabilizing voltage adjustment pin Adjusts the VREG output voltage by connecting an intermediate tap of the external volume (3-pin resistor) connected between the VDD and VREG pins to the RV pin.
XPOFF	5	VREG output ON/OFF control pin Controls S1F76640M0C power-off (VREG output power off) by inputting a control signal from the XPOFF system to this pin.
OSC2	8	Pin connected to oscillation resistor Opened for external clock operation.
OSC1	7	Pin connected to oscillation resistor Functions as a clock input pin for external clock operation
VSS(GND)	6	Power supply pin (Negative side, system GND)

5. FUNCTIONAL DESCRIPTION

① CR oscillation circuit
The S1F76640 is equipped with a CR oscillation circuit as an internal oscillation circuit, connecting external resistor ROSC for oscillation between the OSC1 and OSC2 pins (Fig.5.1).

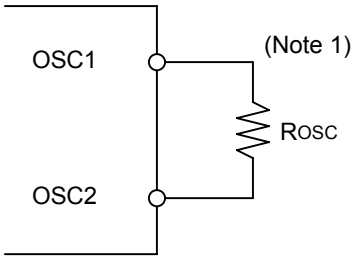


Fig.5.1 CR oscillation circuit

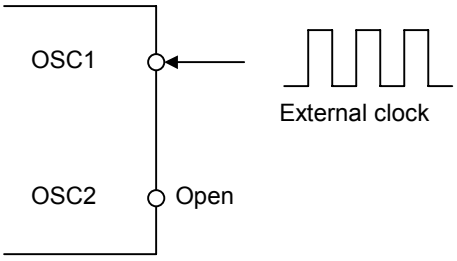


Fig.5.2 External Clock Operation

Note 1: The oscillation frequency varies depending on the wiring capacity, so the wire between the OSC1 and OSC2 pins and ROSC must be short as much as possible.

To set the external resistor ROSC, first obtain the oscillation frequency fOSC that satisfies the maximum efficiency in Figures 7.12 and 7.13, and then obtain ROSC corresponding to the fOSC in Fig.7.1.
The relationship between ROSC and fOSC can be briefly expressed by the following equation on condition that 400kΩ<ROSC<2MΩ.

$$R_{OSC} = A \cdot \frac{1}{f_{OSC}}$$ (where A is a constant: GND = 0V, V_{DD} = 5V, f_{OSC} A = 2.0×10^{10} (Ω•Hz))

Therefore, the ROSC value can be obtained from the relational expression above.
(Recommended oscillation frequency: 10kHz to 30kHz (ROSC: 2MΩ to 680kΩ)

For external clock operation, open the OSC2 pin as shown in Fig.5.2 and input external clocks (duty 50%) from the OSC1 pin.

② Voltage converters (I) and (II)
Voltage converters (I) and (II) perform double boosting and triple boosting for input power voltage V_{DD} using clocks generated in the CR oscillation circuit.
For double boosting, the double input voltage is obtained from the Vout pin by connecting an external pump-up capacitor between CAP1+ and CAP1- and jumpering between CAP2+, CAP3+ and V_{OUT}.
For triple boosting, $3V_{DD}$ is output from the V_{OUT} pin by connecting an external pump-up capacitor between CAP1+ and CAP1- and between CAP2+ and CAP2-, and connecting an external smoothing capacitor between V_{DD} and V_{OUT}.
For quadruple boosting, $3V_{DD}$ is output from the V_{OUT} pin by connecting an external pump-up capacitor between CAP1+ and CAP1- and between CAP2+ and CAP2-, and connecting an external smoothing capacitor between V_{DD} and V_{OUT}.
Figures 5.3, 5.4 and 5.5 show the relationships between input and output voltages, using V_{SS} = 0V and V_{DD} = 5V.

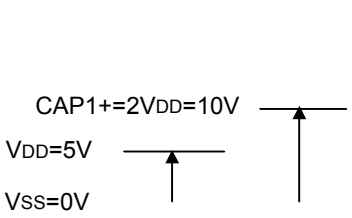


Fig.5.3 Relationships between Double Boosting Voltages

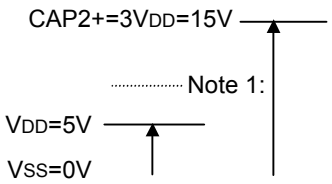


Fig.5.4 Relationships between Triple Boosting Voltages

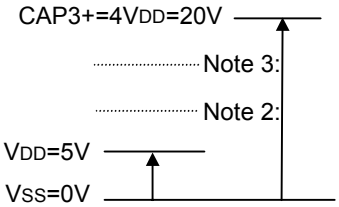
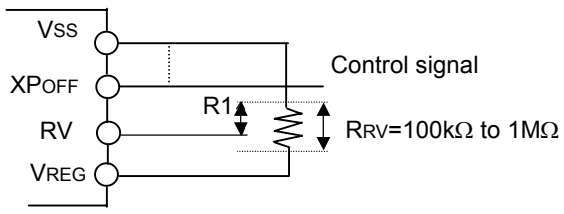


Fig.5.5 Relationships between Quadruple Boosting Voltages

Note 1: In triple boosting, the double boosting output (+10V) cannot be extracted from the CAP2+ pin.
Note 2: In quadruple boosting, the double boosting output (+10V) cannot be extracted from the CAP2+ pin.
Note 3: In quadruple boosting, the triple boosting output (+15V) cannot be extracted from the CAP3+ pin.

③ Reference voltage generator, voltage stabilizer
The reference voltage generator generates a reference voltage required to operate the voltage stabilizer, and provides a temperature gradient to the reference voltage.
There are three types of temperature gradients and the appropriate one is selected by a signal sent from the temperature gradient selection circuit. The voltage stabilizer stabilizes boosting output voltage V_{OUT} and outputs any voltage.
As shown in Fig.5.5, the V_{REG} output voltage can be set to any voltage between the reference voltage V_{RV} and V_{OUT} by connecting the external resistor R_{RV} and changing the voltage of the intermediate tap.



$$V_{REG} = \frac{R_{RV}}{R1} \cdot V_{RV}$$

Fig.5.6 Voltage Stabilizer

The voltage stabilizer, which contains the power-off function, enables V_{REG} output ON/OFF control when the signal is sent from the system (microprocessor, etc.).
When XP_{OFF} = High (V_{DD}), the V_{REG} output is turned on; when XP_{OFF} = Low (GND), it is turned off.
If the V_{REG} output ON/OFF control is not necessary, XP_{OFF} is fixed to High (V_{DD}) as shown in Fig.4.5 (dashed lines).

④ Temperature gradient selection circuit
As shown in Table 5.1, the S1F76640 provides three types of temperature gradients suitable for LCD driving to VREG output.

Table 5.1 Correspondence between Temperature Gradients and VREG Output ON/OFF

XPOFF Note 1)	TC2 Note 1)	TC1 Note 1)	Temperature gradient CT Note 2)	VREG output	CR oscillation circuit	Remarks
1(VDD)	L(VSS)	L(VSS)	-0.40%/°C	ON	ON	—
1(VDD)	L(VSS)	H(VOUT)	-0.30%/°C	ON	ON	—
1(VDD)	H(VOUT)	L(VSS)	-0.50%/°C	ON	ON	—
1(VDD)	H(VOUT)	H(VOUT)	-0.50%/°C	ON	OFF	Serial connection Note 4)
0(VSS)	L(VSS)	L(VSS)	—	OFF(Hi-Z) Note 3)	OFF	—
0(VSS)	L(VSS)	H(VOUT)	—	OFF(Hi-Z) Note 3)	OFF	—
0(VSS)	H(VOUT)	L(VSS)	—	OFF(Hi-Z) Note 3)	OFF	—
0(VSS)	H(VOUT)	H(VOUT)	—	OFF(Hi-Z)	ON	Boosting only Note 5)

Note 1: The high voltage is different between the XPOFF, TC2, and TC1 pins.
Note 2: The temperature gradient CT is defined in the following formula:

$$CT = \frac{V_{REG}(50°C) - V_{REG}(0°C)}{50°C - 0°C} \times \frac{1}{V_{REG}(25°C)} \times 100\ (\%/°C)$$

Example: When CT- = -0.3%/°C is selected;
if VREG output at Ta = 25°C is VREG (25°C) = 8V,
$\Delta V_{REG}/\Delta T = CT \cdot |V_{REG}(25°C)| = -0.3\times10^{-2}\times8 = 24mV/°C$ is obtained,
the $|V_{REG}|$ value reduces 40mV each time the temperature rises by 1°C.
- VREG (25°C) = 10V results in $\Delta|V_{REG}|/\Delta T = 30mV/°C$.

Note 3: When the power is off (VREG output: OFF, CR oscillation circuit: OFF), the VOUT output voltage is set to VDD-0.5V.
Note 4: Selecting this mode for serial connection drives the next-stage IC with the first-stage clock, and reduces the power consumption of the next-stage IC. (See item 8 - (4).)
Note 5: Select this mode for boosting operation only. It minimizes the current consumption.

6. ELECTRICAL CHARACTERISTICS

6.1 Absolute Maximum Ratings

Item	Symbol	Standard value		Unit	Remarks
		Min.	Max.		
Input power voltage	V_{DD}	GND-0.3	24/N 8 6	V	V_{DD} (N= 3, 4) N = 3: Triple boosting N = 4: Quadruple boosting
Input pin voltage	V_I	GND-0.3	V_{DD}-0.3	V	0SC1, XP_{OFF}
		GND-0.3	V_{OUT}-0.3	V	TC1, TC2, RV
Output voltage	V_0	GND-0.3	24	V	V_{OUT} Note 3:
		GND-0.3	V_{OUT}	V	V_{REG} Note 3:
Output pin voltage 1	V_{0C1}	GND-0.3	V_{DD}-0.3	V	CAP1+, CAP2+, 0SC2
Output pin voltage 2	V_{0C2}	GND-0.3	2×V_{DD}-0.3	V	CAP1-
Output pin voltage 3	V_{0C3}	GND-0.3	3×V_{DD}-0.3	V	CAP2-
Output pin voltage 4	V_{0C4}	GND-0.3	4×V_{DD}-0.3	V	CAP3-
Allowable dissipation	Pd	—	210	mW	SSOP-16PIN
Operating temperature	T_{opr}	-40	85	°C	—
Storage temperature	T_{stg}	-55	150	°C	—
Soldering temperature and time	T_{sol}	—	260•10	°C•s	Lead part

Note 1: Use exceeding the absolute maximum ratings above may cause a permanent destruction of the IC. A long-duration operation at the absolute maximum ratings may significantly decrease reliability.

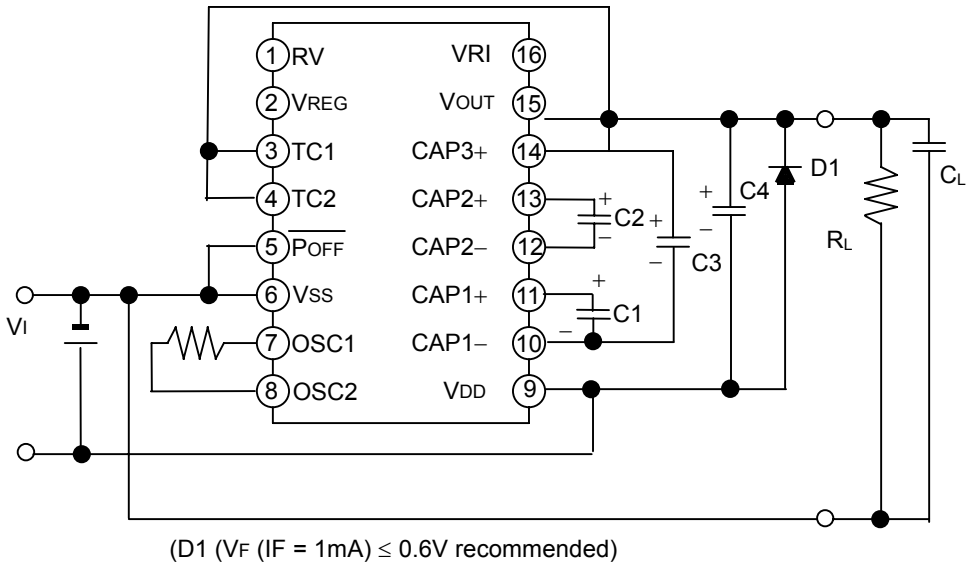
Note 2: All the voltage values above are based on GND.

Note 3: The V_{OUT} and V_{REG} output pins output the boosted voltage and stabilized boosted-voltage. No external voltage should therefore be applied to these pins. When being compelled to apply external voltage to the pins for use, it must be in the allowable range of the rated voltages above.

6.2 Recommended Operating Conditions

Item	Symbol	Standard value		Unit	Remarks
		Min.	Max.		
Boosting start voltage	VSAT1	1.8	—	V	ROSC=1MΩ, C4≥10μF CL/C4≥1/20, Note 2)
	VSAT2	2.2	—	V	ROSC=1MΩ
Boosting stop voltage	VSTP	—	1.8	V	ROSC=1MΩ
Output load current	IOUT	—	20	mA	—
Oscillation frequency	fOSC	10	30	kHz	—
External resistor for oscillation	ROSC	680	2000	kΩ	—
Boosting capacitor	C1,C2,C3,C4	3.3	—	μF	—
Stabilization-output adjusting resistor	RRV	100	1000	kΩ	—

Note 1: All voltages are based on the condition that the VSS (GND) is equal to 0V.
Note 2: For low-voltage (VDD = 1.8 to 2.2V) operation, the recommended circuit is as follows:



(D1 (VF (IF = 1mA) ≤ 0.6V recommended)

Fig.6.2.1 Recommended Circuit for Low-voltage Operation (Example of Quadruple Booster Circuit)

6.3 Electrical Characteristics

If not specified Ta=-40°C to +85°C V_{SS}=0V、V_{DD}=5V

Item	Symbol	Standard value			Unit	Conditions	Measuring circuit
		Min.	Typ.	Max.			
Input power voltage	V_{DD}	1.8	—	5.5	V		—
Output voltage	V_{OUT}	—	—	22	V		—
	V_{REG}	VRV	—	22	V	R=∞, R_{RV}=1MΩ, V_{OUT}=22V	②
Stabilizer operating voltage	V_{OUT}	VRV+2.5	—	22	V		—
Booster current consumption	I_{opr1}	—	30	60	μA	RL=∞, R_{OSC}=1MΩ	①
Stabilized circuit current consumption	I_{opr2}	—	25	50	μA	RL=∞, V_{OUT}=20V	②
Static current	IQ	—	—	2	μA	TC2=TC1=V_{OUT}, RI=∞	①
Oscillation frequency	f_{0SC}	14.0	17.5	21.0	kHZ	R_{OSC}=1MΩ	①
Output impedance	R_{OUT}	—	250	350	Ω	I_{OUT}=10mA	①
Boosting power conversion efficiency Note 2)	Pef	90	95	—	%	I_{OUT}=5mA	①
Stabilization output voltage variation	ΔV_{REG} $\Delta V_{OUT} \cdot V_{REG}$		0.1	—	%/V	10V<V_{OUT}<20V, V_{REG}=10V RL=∞, Ta=25°C	②
Stabilization output load variation Note 3)	ΔV_{REG} ΔI_{OUT}	—	5	—	Ω	V_{OUT}=20V, V_{REG}=15V Ta=25°C, 0<I_{OUT}<10Ma TC1=V_{OUT}, TC2=GND	②
Stabilization output saturated resistance Note 4)	R_{SAT}	—	10	—	Ω	RSAT=Δ(V_{OUT}-V_{REG})/ ΔI_{OUT} 0<I_{OUT}<10mA, RV=GND, Ta=25°C	②
Reference voltage	V_{RV0}	1.70	1.90	2.20	V	TC2=GND, TC1=V_{OUT}, Ta=25°C	②
	V_{RV1}	1.80	2.00	2.20	V	TC2=TC1=GND,Ta=25°C	
	V_{RV2}	1.50	1.60	1.80	V	TC2=V_{OUT}, TC1=GND, Ta=25°C	
Temperature gradient	CT0	-0.40	-0.30	-0.20	%/°C	V_{DD}=5V、V_{OUT}=20V Note 5)	②
	CT1	-0.50	-0.40	-0.30	%/°C		
	CT2	-0.60	-0.50	-0.40	%/°C		
Input leak current	IL	—	—	2	μA	Poff, TC1, TC20SC1, and RV pins	③

Note 1: All voltages are based on the condition that the V_{SS} (GND) is equal to 0V.

Note 2: The values above indicate the conversion efficiency of the booster. When the stabilizer is active, the loss is (V_{REG} - V_{OUT}) × I_{OUT}.
It is, therefore, recommended to use the method of reducing (V_{OUT} - V_{REG}) as much as possible.
If (V_{OUT} - V_{OUT}) × I_{OUT} is high, the stabilizer characteristics vary as the IC temperature rises.

Note 3: See Figures 7.15, 7.16, and 7.17.

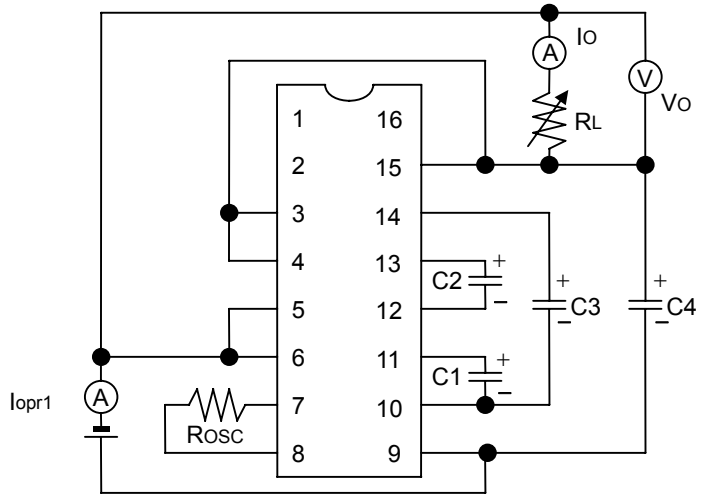
Note 4: RSAT indicates the inclination shown in Fig.7.18; V_{OUT} - Δ(V_{OUT} - V_{REG}) indicates the lower limit voltage of the V_{REG} output.

Note 5: The computational expression of CT is shown below:

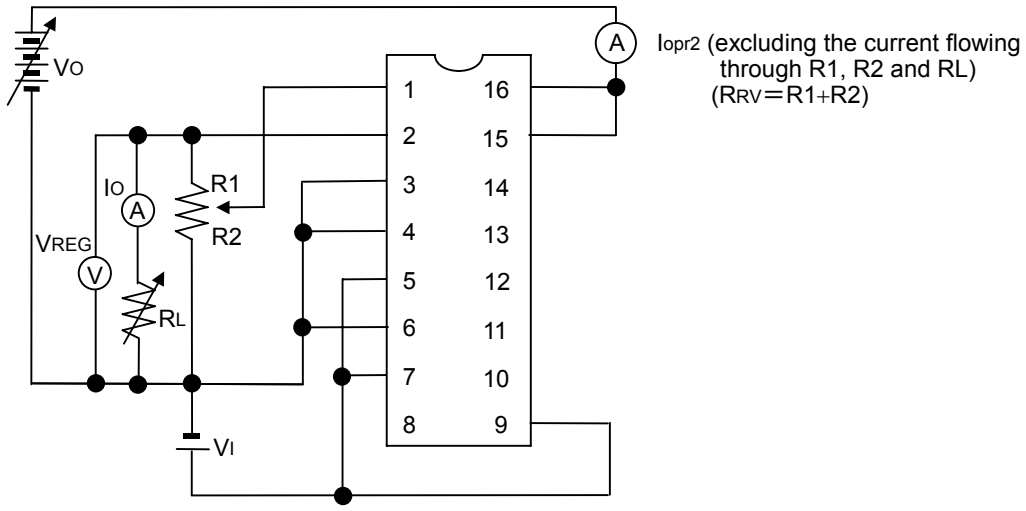
$$CT = \frac{V_{REG}(50°C) - V_{REG}(0°C)}{50°C - 0°C} \times \frac{1}{V_{REG}(25°C)} \times 100\ (\%/°C)$$

6.4 Measuring Circuit

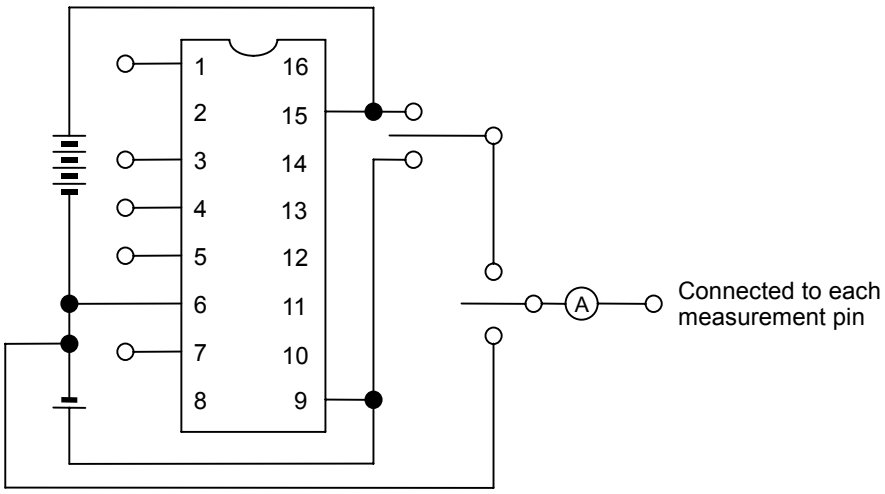
① Booster circuit characteristics Measuring circuit



② Stabilization circuit characteristics Measuring circuit



③ Input leak current Measuring circuit



7. CHARACTERISTIC DATA

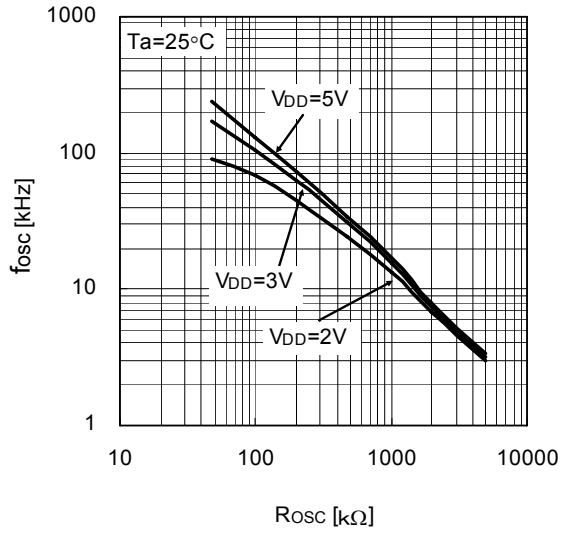


Fig.7.1 Oscillation frequency- External resistor for oscillation

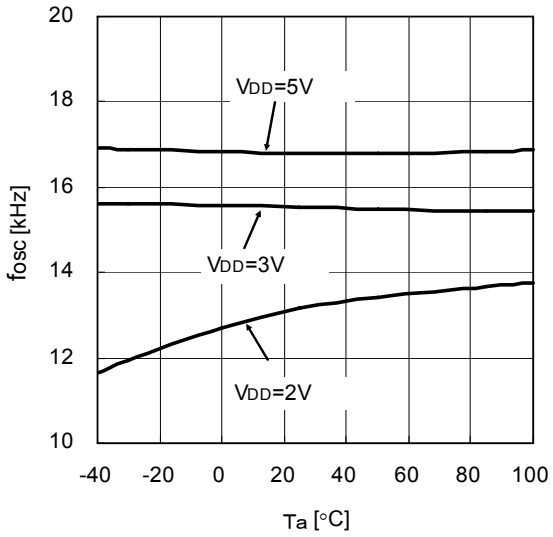


Fig.7.2 Oscillation frequency

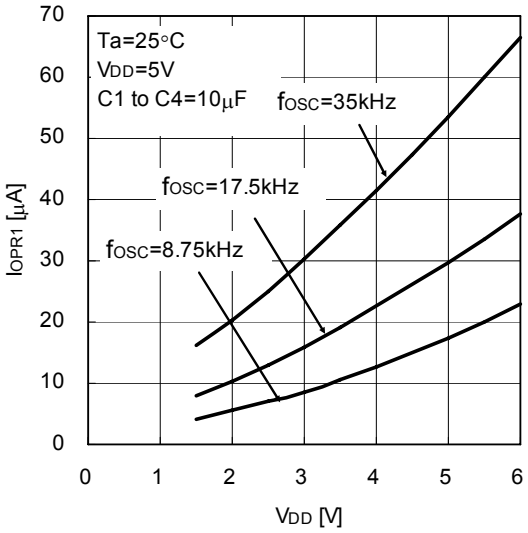


Fig.7.3 Booster current consumption - Input voltage

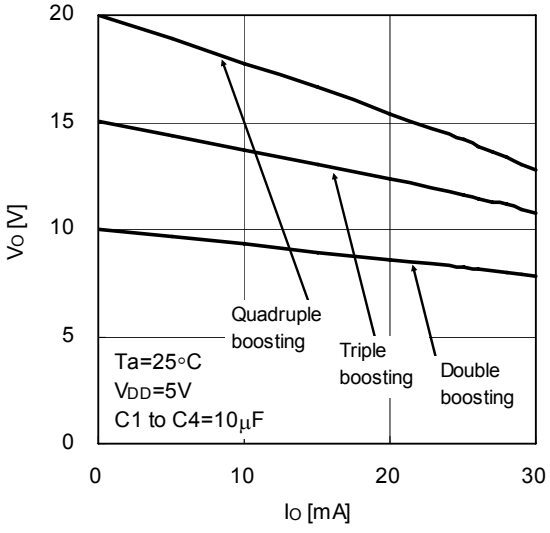


Fig.7.4 Output voltage (VO) - Output current ①

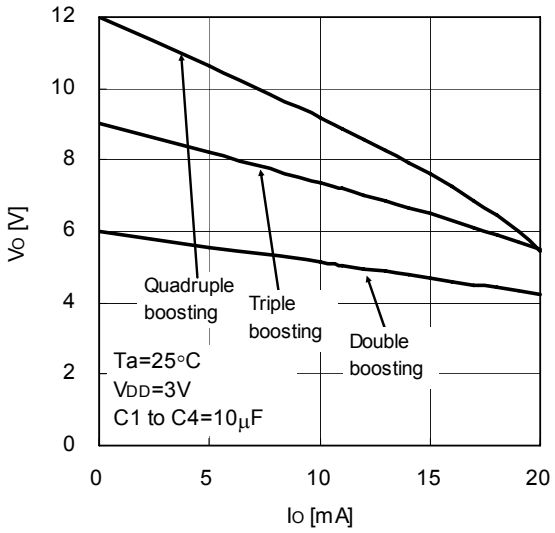


Fig.7.5 Output voltage (VO) - Output current ②

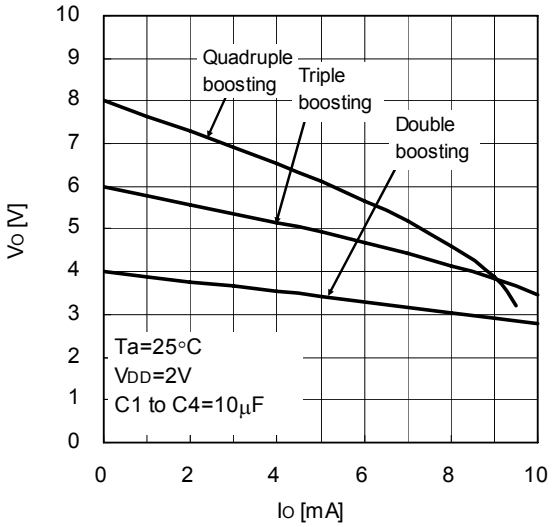


Fig.7.6 Output voltage (VO) - Output current ③

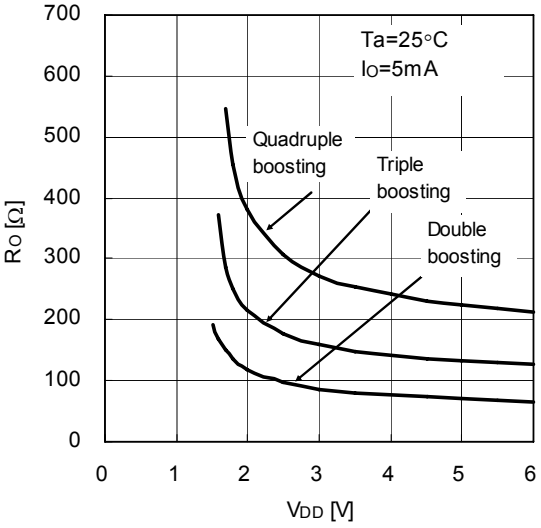


Fig.7.7 Output impedance - Input voltage ①

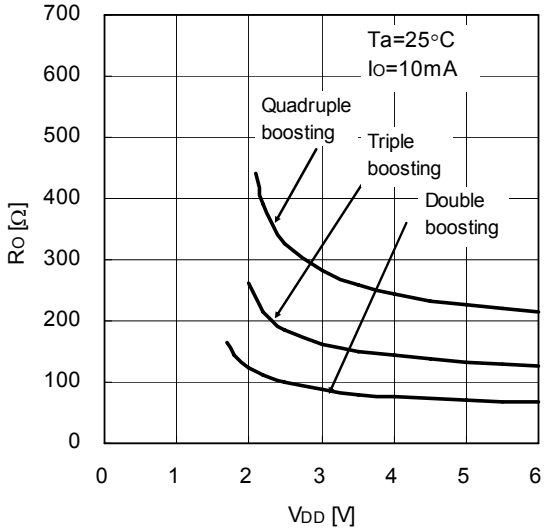


Fig.7.8 Output impedance - Input voltage ②

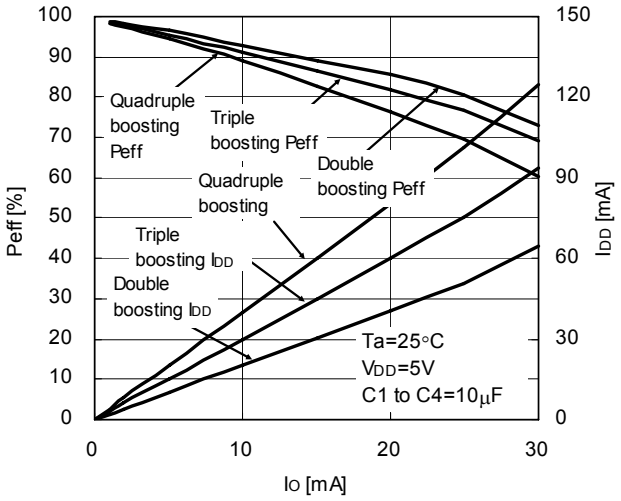


Fig.7.9 Boosting power conversion efficiency - Output current ①
Input current - Output current ①

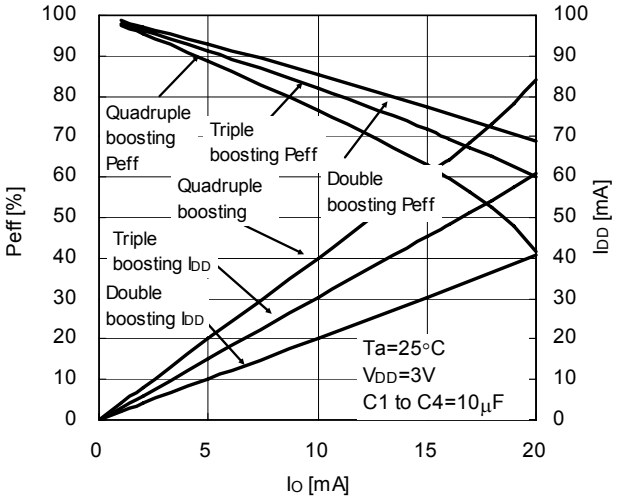


Fig.7.10 Boosting power conversion efficiency - Output current ②
Input current - Output current ②

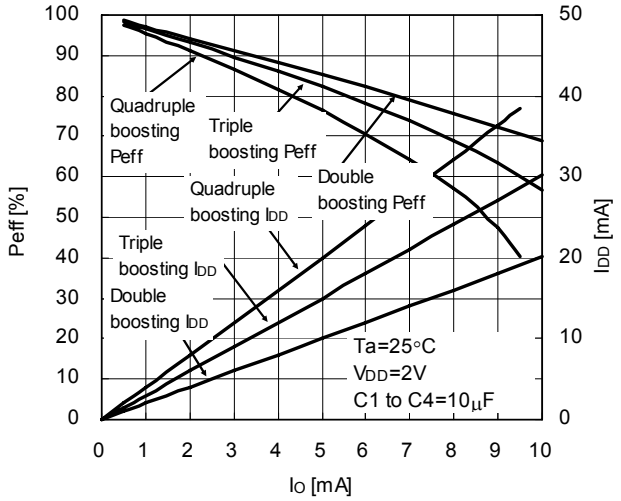


Fig.7.11 Boosting power conversion efficiency - Output current ③
Input current - Output current ③

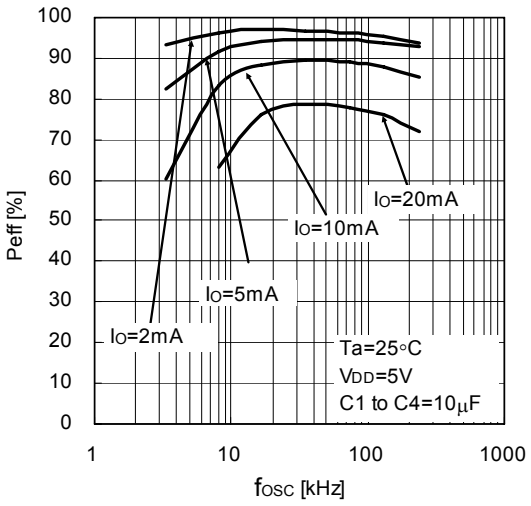


Fig.7.12 Boosting power conversion efficiency - Oscillation frequency ①

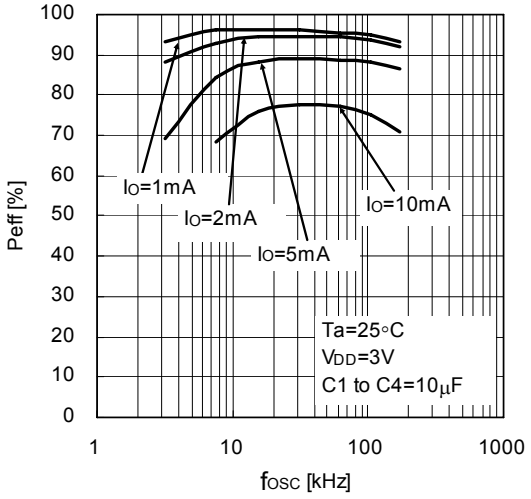


Fig.7.13 Boosting power conversion efficiency - Oscillation frequency ②

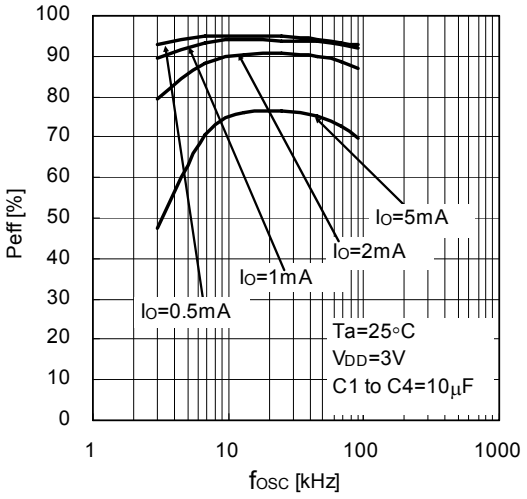


Fig.7.14 Boosting power conversion efficiency - Oscillation frequency ③

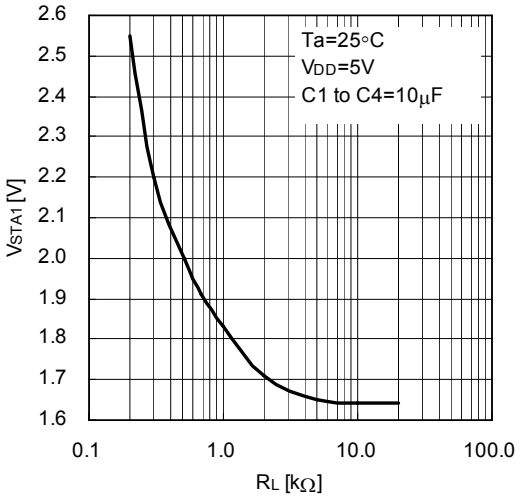


Fig.7.15 Boosting start voltage - load resistance

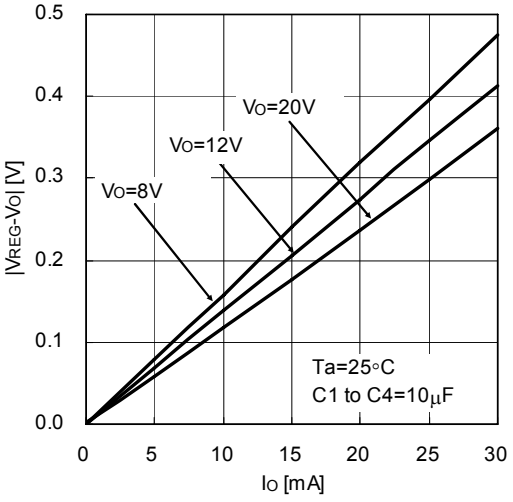


Fig.7.16 Stabilization output saturated resistance - Load current

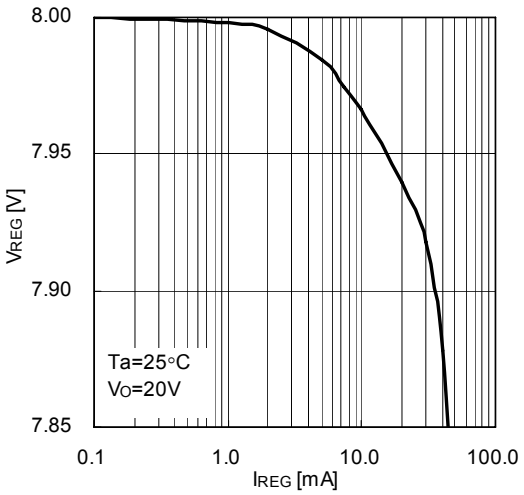


Fig.7.17 Output voltage (V_{REG}) - Output current ①

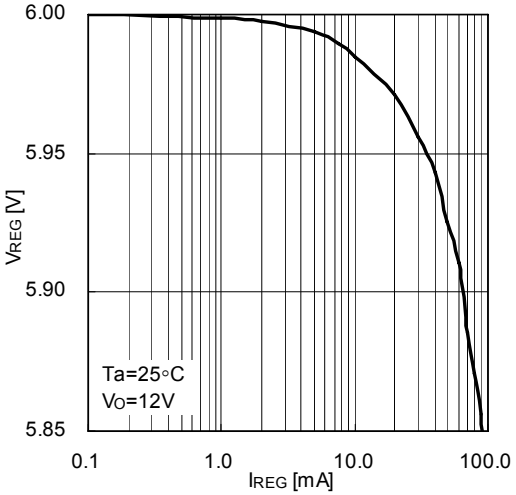


Fig.7.18 Output voltage (V_{REG}) - Output current ②

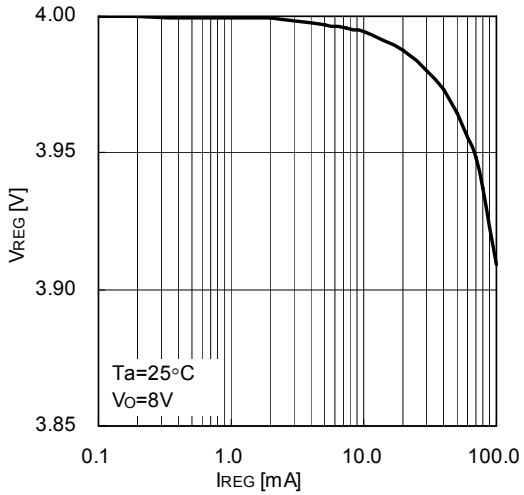


Fig.7.19 Output voltage (V_{REG}) - Output current ③

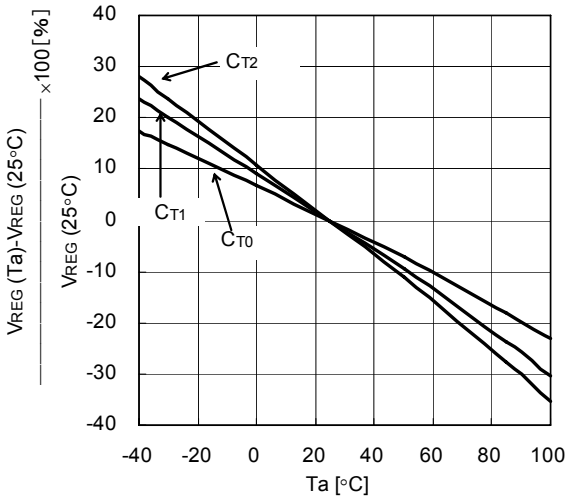


Fig.7.20 Reference voltage - Temperature

8. APPLIED CIRCUIT EXAMPLES

(1) Quadruple boosting, Triple Boosting and Double Boosting

Fig.8.1 shows a connection example for obtaining quadruple boosting output for input voltage by operating the booster only.

For triple boosting, remove the capacitor C1 and jumper between the CAP1+ (pin No.11) and VDD (No.9) pins; triple boosting (15V) is obtained from VOUT.

For double boosting, further remove the capacitor C2 and jumper between the CAP2+ (pin No.13) and VDD (No.9) pins; double boosting (10V) is obtained from VOUT.

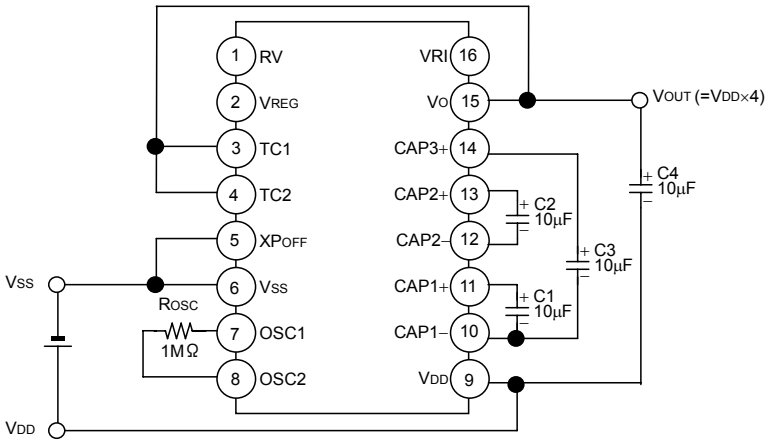


Fig.8.1 Quadruple Booster

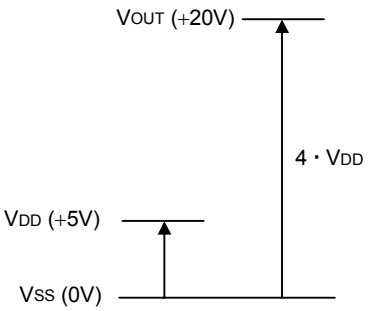


Fig.8.2 Diagram of Voltage Relations for Quadruple Boosting

(2) Quadruple boosting + Stabilizer

Fig.8.3 shows an applied-circuit example for stabilizing the boosting output obtained in Fig.8.1 the stabilizer and providing the temperature gradient for the VREG output through the temperature gradient selection circuit.

This application example can indicate two outputs from VO and VREG at the same time.

Triple boosting + stabilizer operation using the triple boosting and double boosting + stabilizer operation is also available.

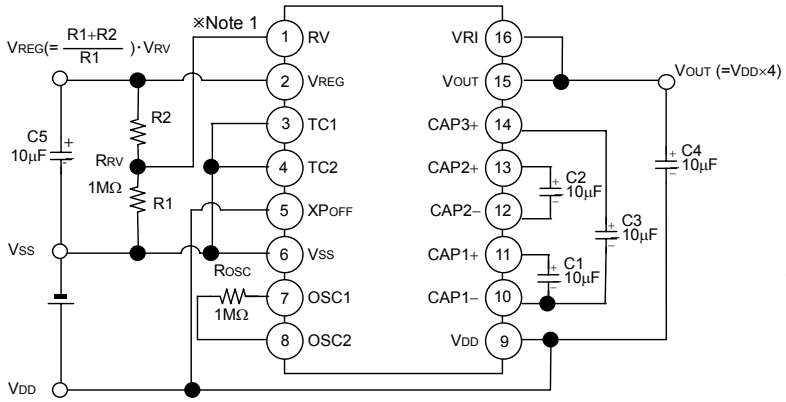


Fig.8.3 Quadruple Boosting + Stabilizer (Temperature Gradient of CT1)

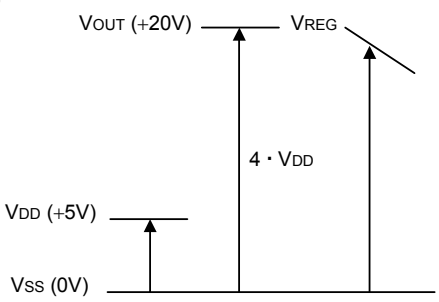


Fig.8.4 Diagram of Voltage Relations for Quadruple Boosting + Stabilizer

Note 1: The RV pin (No.1) has high input impedance. If the wire is long, use a shield wire or the like to prevent noise. To reduce the influence of noise, it is effective to reduce the RRV value. (However, the RRV current consumption will increase.)

(3) Parallel Connection

As shown in Fig.8.1, multi-connection reduces output impedance Ro.
Therefore, a configuration of n parallel connections lowers Ro to 1/n. Smoothing capacitor C4, which is a single device, is shared by those connections. To obtain stabilization output after parallel connections, apply the connection shown in Fig.8.3 to only one of the n parallel connections shown in Fig.8.5.

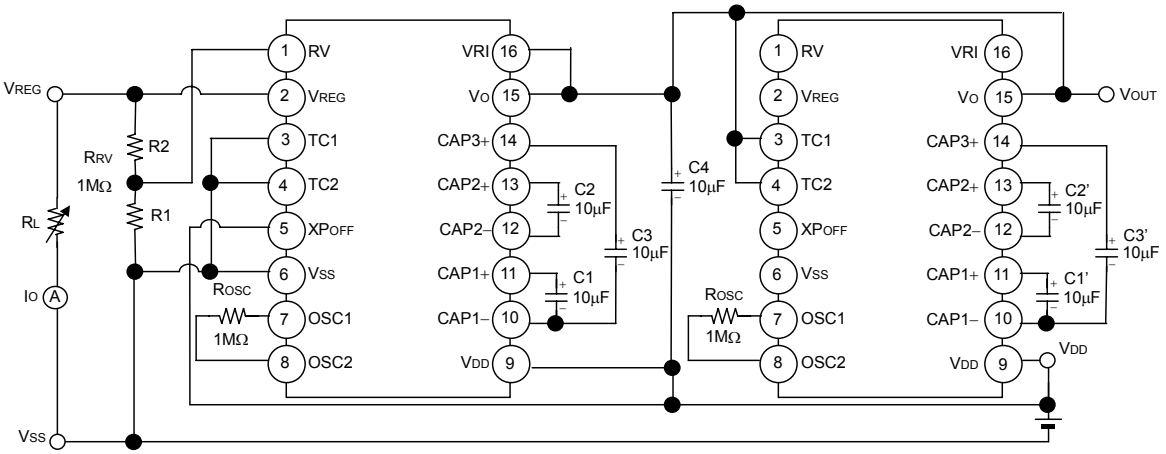


Fig.8.5 Parallel Connection

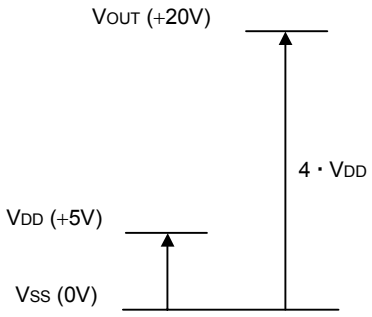


Fig.8.6 Diagram of Voltage Relations in Parallel Connection

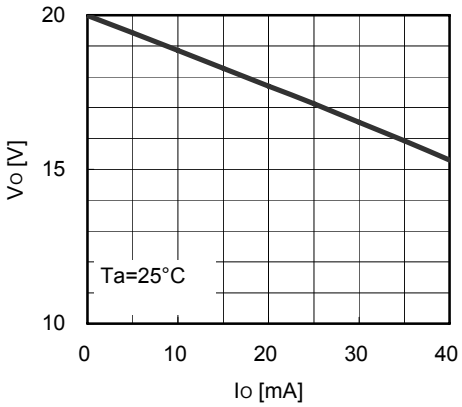


Fig.8.7 Output Voltage - Output Current

(4) Serial Connection

The serial connection in the S1F76640 (connecting V_{DD} and V_O in the pre-stage to V_{SS} and V_{DD} in the next stage respectively) further increases output voltage. However, the serial connection raises output impedance. Fig.8.8 shows an example of serial connection for further stabilizing output by obtaining V_O = 25V from V_{DD} = 5V.

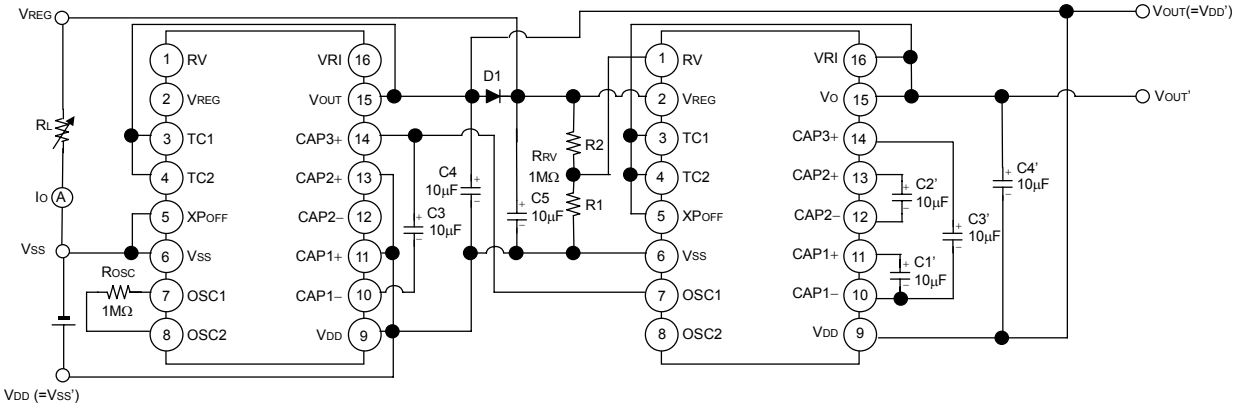


Fig.8.8 Serial Connection

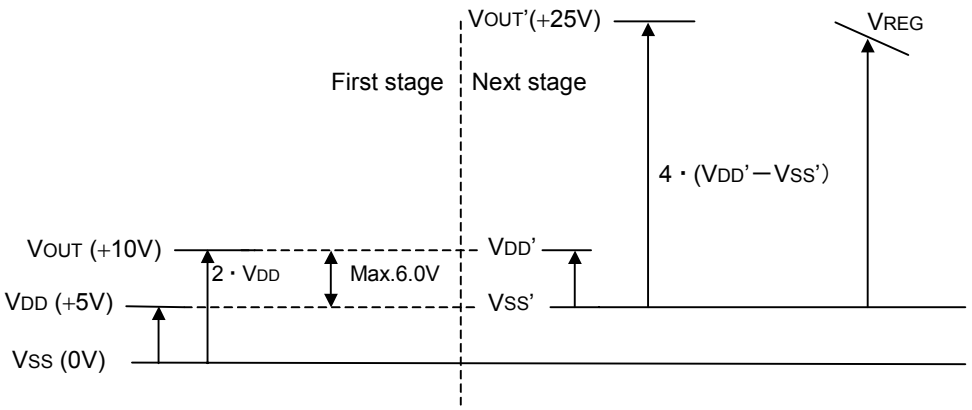


Fig.8.9 Diagram of Voltage Relations in Serial Connection

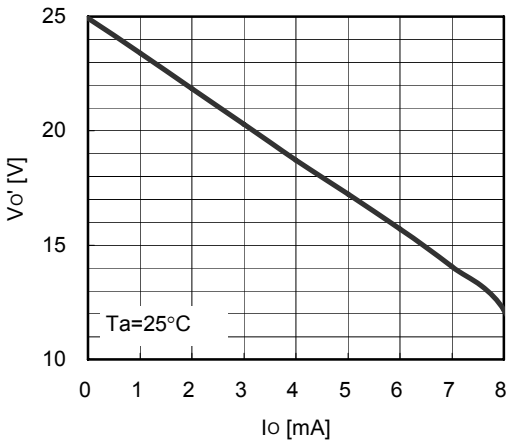


Fig.8.10 Output Voltage - Output Current

Note 1: <Notes on load connection>
As shown in Fig.8.8, when connecting load between VSS in the first stage (or other voltage below VSS in the second stage) and VREG in the second stage in serial connection, the following points should be noted: When the IC is activated or no normal output is generated at the VREG pin while VREG is turned off by the POFF signal, current flows into to the VREG pin from VSS in the first stage (or other voltage below VSS in the second stage) through load. If the voltage exceeding the absolute maximum rating below VSS in the second stage is generated at the VREG pin, the may interfere with normal operation of the IC. For serial connection, as shown in Fig.8.8, connect diode D1 between VDD in the second stage and VREG, so that the voltage below VSS in the second stage will not be applied to the VREG pin.

Note 2: In Fig.8.8, the first stage is assigned to triple boosting and the next-stage to quadruple boosting; however, quadruple boosting is available for both the first and next stages unless the input voltage VDD' - VSS' in the next stage exceeds the standard value (6.0V). For serial connection, each IC must be designed in compliance with the standard (VDD - VSS ≤ 6.0V, VO - VSS ≤ 24V) (See Fig.8.9).

Note 3: When double boosting is provided in the first stage, the first-stage CAP1- output can be used as a next-stage clock; however, when triple boosting is provided, it cannot be used as a next-stage clock. Therefore, to obtain a next-stage clock, externally install ROSC and use an internal oscillator. As shown in Table 4.2, the next-stage external clock operation by the pre-stage CAP1- output is available only for temperature gradient CT = -0.5%/°C. If another temperature gradient is required, use an internal oscillator like the above.

Note 4: In serial connection, the temperature gradient is provided for the VSS - VREG voltage (VREG – VSS' in Fig.8.9) of the IC in which the stabilizer is active.
The VREG value changes according to temperature as follows:

$$\frac{\Delta \mid V_{REG} \mid}{\Delta T} \; CT \; (\; V_{REG} \; (25°C) - V_{SS}' \;)$$

It changes at the ratio above.

(5) Negative Voltage Conversion

The S1F76640 converts input voltage to negative voltage for double boosting or triple boosting through the circuit shown in Fig.8.11. (For double boosting, remove capacitor C2 and diode D3 and jumper between both ends of D3.)

However, the output voltage rises forward voltage VF of the diode. For example, as shown in Fig.8.12, V_{SS} =0V; V_{DD} = 5V; and V_F = 0.6V results in V_O' = -10V+3×0.6V = - 8.2V (-5V+2×0.6V = -3.8V for double boosting).

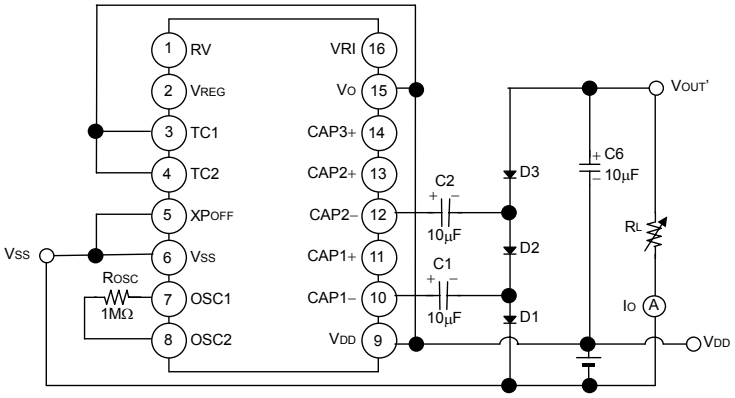


Fig.8.11 Negative-Voltage Conversion

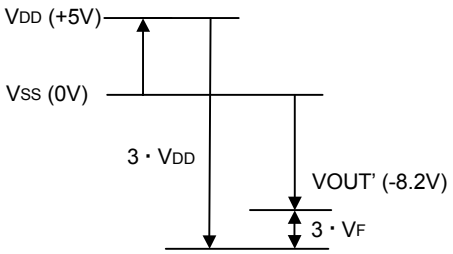


Fig.8.12 Diagram of Voltage Relations for Negative Voltage Conversion

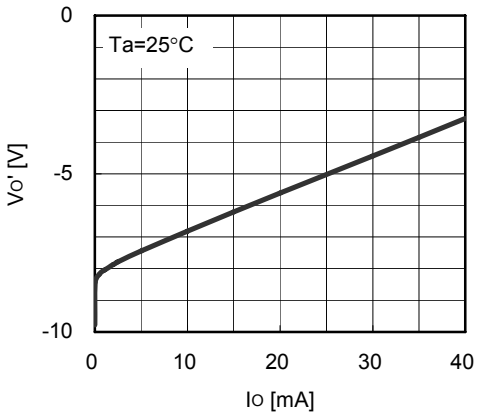


Fig.8.13 Output Voltage - Output Current

(6) Negative-Voltage Conversion + Positive-Voltage Conversion
Combining the triple boosting (Fig.8.1) with the negative voltage conversion (Fig.8.11) generates the circuit shown in Fig.8.14, and outputs 15V and -8.2V from 5V input.
In this case, the output impedance is higher than that for negative voltage conversion only or positive voltage conversion only.

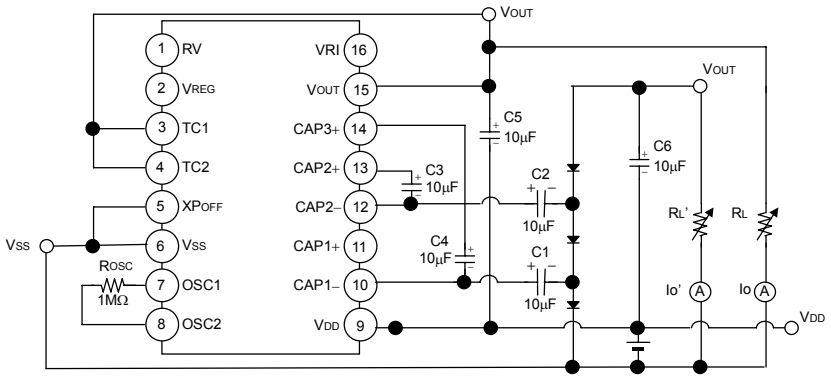


Fig.8.14 Negative-Voltage Conversion + Positive-Voltage Conversion

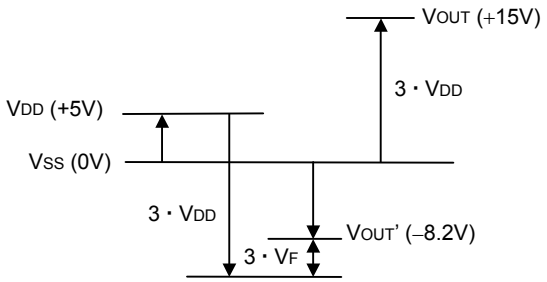


Fig.8.15 Diagram of Voltage Relations for Negative-Voltage Conversion + Positive-Voltage Conversion

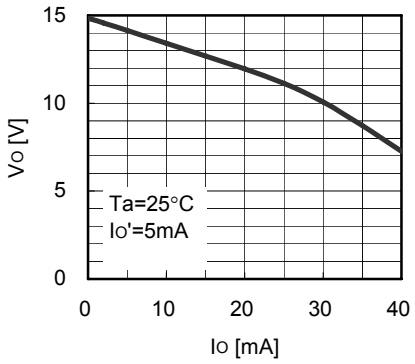


Fig.8.16 Output Voltage - Output Current

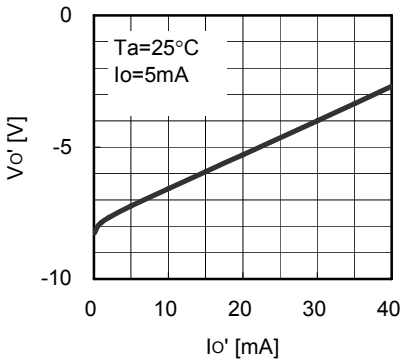


Fig.8.17 Output Voltage - Output Current

(7) Example of Changing the Temperature Gradient with an External Temperature Sensor (Thermistor)
The S1F76640, which is equipped with the temperature gradient selection circuit in the stabilizer, enables you to select three types of temperature gradients (-0.30%/°C, -0.40%/°C, and -0.50%/°C) as VREG output. If other temperature gradients are required, as shown in Fig.8.18, connect a thermistor to resistor RRV (for output voltage adjustment) in series; you can change the temperature gradient to any value.

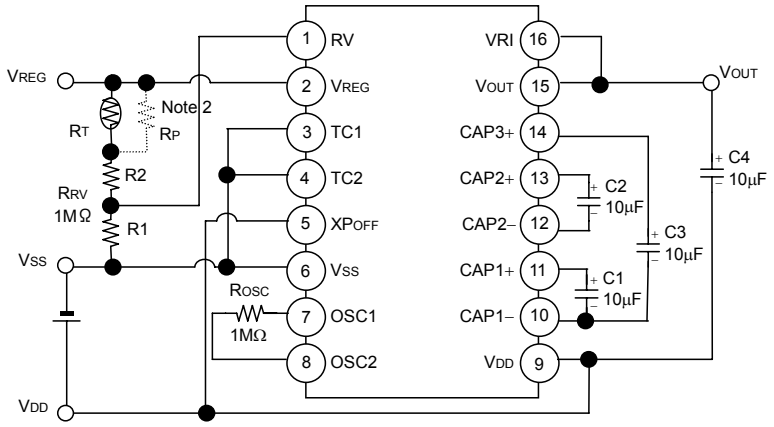
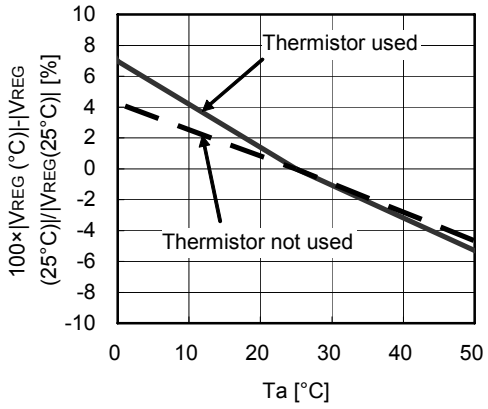


Fig.8.18 Temperature Gradient Change Example

(For pins 3 and 4, select a lower temperature gradient than the one to be changed from Table 5.1.)



[Measurement conditions]
VDD: 5V
VSS: 0V
RRV: 1MΩ (set to VREG = 10 at 25°C)
RT: 10kΩ (0°C/50°C Ratio 9.00)
Temperature gradient: -0.3 %/°C

Fig.8.19 Output Voltage - Temperature

Note 1: The relationship between RT and VREG is indicated as follows:

$$V_{REG} = \frac{R_{PV} + R_T}{R1} R_V$$

Using a thermistor as RT increases the temperature gradient for VREG.

Note 2: The temperature characteristics of the thermistor indicate the nonlinearity; however, connecting resistor RP to the thermistor in parallel changes nonlinear characteristics to linear characteristics.

(8) Example of Configuration of Electronic Volume Circuit of Voltage Stabilization Output (VREG)

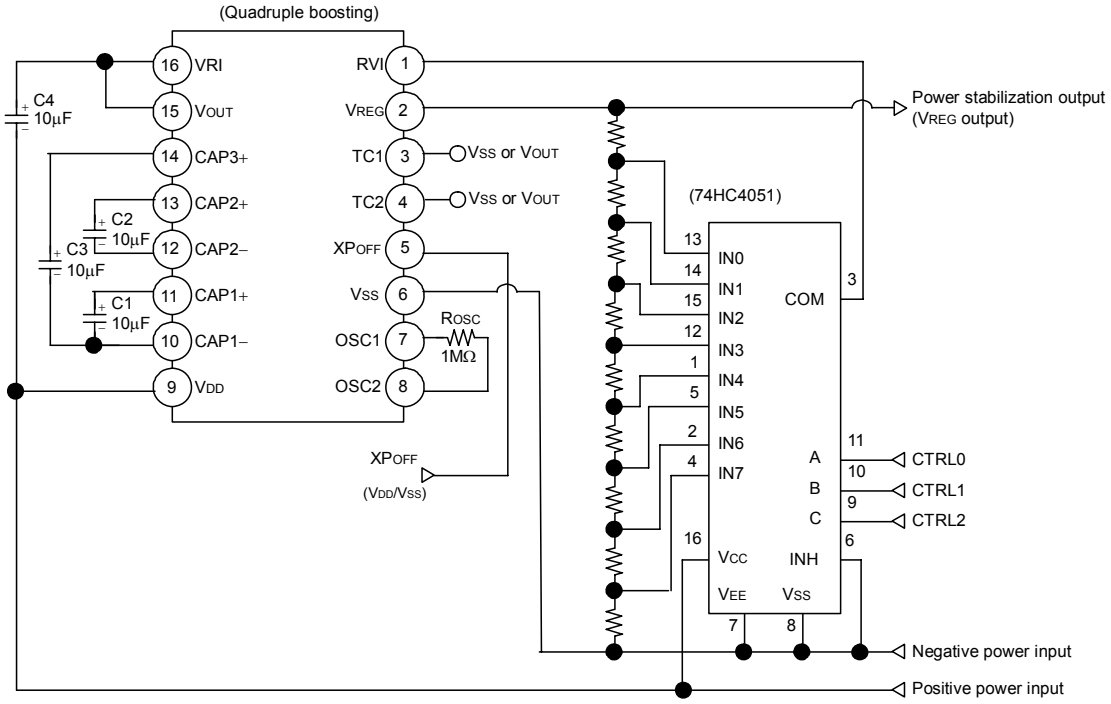


Fig.8.20 Electronic Volume Circuit of Voltage Stabilization Output

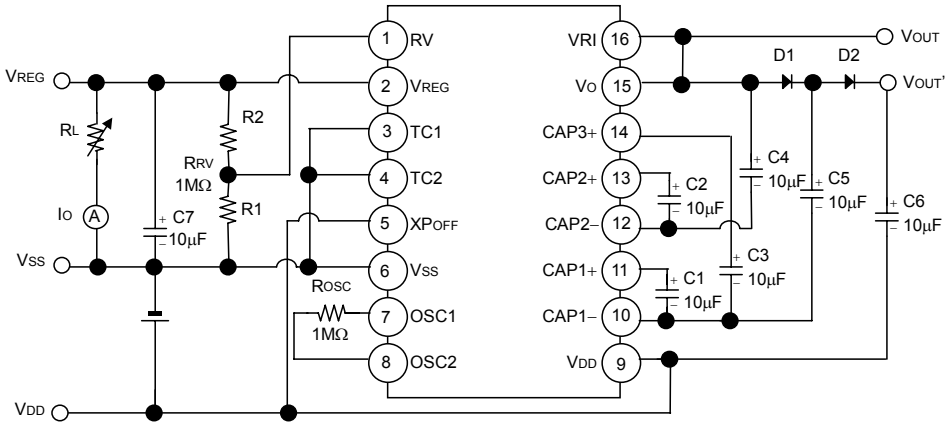
(9) Example of Configuration of Booster Circuits of High Magnification Using Diode

Adding an external diode to the S1F76640 provides quintuple or higher boosting operation and voltage stabilization output. It is recommended to use the diode of smaller V_F as the output impedance of the boosting output increases due to the influence of drop of forward voltage V_F of the diode. V_{DD} = 4V and V_F = 0.6V results in output shown in Fig.8.22.

Fig.8.21 shows an example of circuit configuration that provides boosting by 6x magnification using two diodes and voltage stabilization output. Use the shortest possible wire between V_O and VRI.

Fig.8.22 shows the diagram of voltage relations.

Use the voltage to be applied to the VRI pin at or below the absolute maximum rated voltage.



(For pins 3 and 4, select any temperature gradient.)

Fig.8.21 Boosters of High Magnification

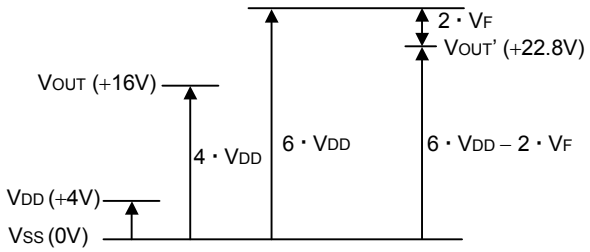


Fig.8.22 Diagram of Voltage Relations of Boosters of High Magnification

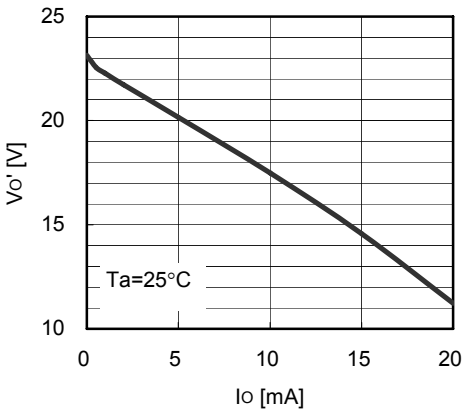


Fig.8.23 Output Voltage - Output Current

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